## REMARKS/ARGUMENTS

Claims 1-26 are pending in the application. Claims 1-26 remain in the application. Claims 14 and 17-18 have been amended for purposes of clarity.

Claims 7-13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kahle et al., U.S. Patent No. 5,956,495 (hereinafter "Kahle") in view of McCrocklin et al, U.S. Patent No. 4,761,733 (hereinafter "McCrocklin"). Claims 1-6 and 14-26 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kahle in view of McCrocklin in view of Shiell, U.S. Patent No. 5,864,697 (hereinafter "Shiell").

## Claim Rejections under 35 U.S.C.§ 103

Claims 7-13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kahle et al., U.S. Patent No. 5,956,495 (hereinafter "Kahle") in view of McCrocklin et al, U.S. Patent No. 4,761,733 (hereinafter "McCrocklin"). Kahle generally discloses a series of guest instructions including at least one guest branch instruction and other guest instructions stored in memory (*See* Kahle, Abstract). McCrocklin discloses a direct-execution microprogrammable microprocessor system with an emulatory microprogrammable microprocessor for direct execution of microinstructions in main memory through a microinstruction port (*See* McCrocklin, Abstract).

Applicants respectfully submit that neither Kahle, McCrocklin, nor any combination thereof disclose predicting whether a first micro-op is a bogus branch instruction, as recited in claims 7 and 10. McCrocklin does not disclose this element, and the Office Action does not claim such. Kahle states:

SJO 46777-1 9

Returning to block 226, in response to a determination that V<sub>B</sub> field 134 is not marked valid in the entry 110 being examined, the process proceeds to block 230. Block 230 depicts guest branch unit 80 predicting the branch by reference to conventional branch history table (BHT) 82. PTF 144 is set to 1 to indicate that the branch was predicted taken and is cleared (set to 0) to indicated that the branch was predicted not taken. The process then proceeds from block 230 to block 260, which illustrates guest branch unit 80 calculating the address of the predicted path and transmitting the address to data cache 34 via instruction prefetch unit 74. In order to permit recovery from misprediction, the address of the non-predicted path is stored in other path register 81, as illustrated at block 262. As depicted at block 264, all subsequent guest instructions are marked as speculative while the guest branch instruction remains unresolved by setting S field 126 in the appropriate entries 110 of guest instruction queue 100. The process thereafter terminates at block 280.

(Kahle, Col. 10, lines 34-67).

In other words, Kahle describes determining whether of a branch has been predicted to be taken or not taken, as opposed to determining if a branch instruction is bogus, as required by claims 7 and 10. For example, a bogus branch is described as a branch that is predicted to occur at an address that does not contain a branch or will have a target address that is invalid. Therefore claims 7 and 10 are not obvious under Kahle in view of McCronklin. In addition, Applicants respectfully submit that claims 8-9 and 11-13 are allowable as depending from allowable base claims 7 and 10. Accordingly reconsideration and withdrawal of the rejection of claims 7-13 under 35 U.S.C. §103(a) is respectfully requested.

Claims 1-6 and 14-26 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kahle in view of McCrocklin in view of Shiell, U.S. Patent No. 5,864,697 (hereinafter "Shiell"). Shiell discloses a microprocessor using combined actual branch history and speculative branch history to predict branches (*See* Shiell, Abstract).

Applicants respectfully submit that neither Kahle, McCrocklin, Shiell, nor any combination thereof disclose predicting whether a first micro-op is a bogus branch

SJO 46777-1 10

instruction, as recited in claims 7 and 10. As shown above, Kahle and McCrocklin does not disclose this element. Further, Shiell does not disclose this element, and the Office Action does not claim such.

Therefore claims 1 and 19 are not obvious under Kahle in view of McCronklin and in further view of Shiell. In addition, Applicants respectfully submit that claims 2-6 and 20-26 are allowable as depending from allowable base claims 1 and 19. Accordingly reconsideration and withdrawal of the rejection of claims 1-6 and 19-26 under 35 U.S.C. §103(a) is respectfully requested.

Applicants respectfully submit that neither Kahle, McCrocklin, Shiell, nor any combination thereof disclose removing entries from a branch prediction logic storage buffer that may later produce bogus branches, as recited in claim 14. As shown above, Kahle, McCrocklin and Shiell do not disclose bogus branches in any way.

Therefore claim 14 are not obvious under Kahle in view of McCronklin and in further view of Shiell. In addition, Applicants respectfully submit that claims 15-18 are allowable as depending from allowable base claim 14. Accordingly reconsideration and withdrawal of the rejection of claims 14-18 under 35 U.S.C. §103(a) is respectfully requested.

In light of the arguments above, reconsideration and withdrawal of claims 1-26 under U.S.C. §103(a) is respectfully requested.

SJO 46777-1 11

## **CONCLUSION**

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Dated: June 21, 2004

By:

Stephen T. Neal (Reg. No. 47,815)

Attorneys for Intel Corporation

KENYON & KENYON 333 W. San Carlos Street Suite 600 San Jose, CA 95110

Telephone:

(408) 975-7500

Facsimile:

(408) 975-7501